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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,056	WILLE ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-27,29-45 and 47-97* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-27,29-45 and 47-97* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6, 11, 13-18, 24, 27, 29-36, 42, 45, 47-49, 52-57, 62-64, 66-69, and 77-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein et al. (U.S. Patent No. 6,365,529), in view of Tsai et al. (U.S. Patent No. 6,878,615).

4. As to claim 1, Hussein discloses a method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of: depositing a thin film (103) on the substrate (100) (column 4, lines 51-53; Figure 1B); depositing a layer of planarizing material (104) on the thin film (103) (column 5, lines 43-51; Figure 1D);

depositing a layer of anti-reflective coating (108) (column 10, lines 46-47, lines 55-60); depositing at least one layer of imaging material (136) (column 6, lines 65-67; Figure 3C); forming at least one first pattern shape (106) in the layers of imaging material (136), anti-reflective coating (108) and planarizing material (104) (column 11, lines 19-22; Figures 1E-F); removing the imaging material (136), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 23-24); removing the anti-reflective coating (108), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 31-35); and transferring the first pattern shape to the thin film (103) (column 11, lines 19-22; Figures 1E-F).

5. Hussein does not expressly disclose depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material. Hussein discloses the use of both an imaging material (136) (column 6, lines 65-67) and low-k dielectric thin film (103) (column 4, lines 60-67). Tsai teaches that outgassing from a low-k dielectric film interacts with the imaging layer, resulting in the poisoning of via holes (column 5, lines 1-15; column 6, lines 12-28). To prevent poisoning, Tsai further teaches depositing a layer of barrier material (250) (column 6, lines 34-44; Figure 2C) that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material (column 5, lines 10-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material and to modify Hussein's method to

account for the barrier material. One who is skilled in the art would be motivated to prevent the deleterious effects of via poisoning.

6. As to claim 2, Hussein discloses that at least one second pattern shape (107) is formed in the thin film (103) prior to depositing the layer of planarizing material (104) (column 5, lines 14-15), and the second pattern shape (107) is filled by the planarizing material (104) (column 5, lines 43-45).

7. As to claim 3, Hussein discloses that the thin film (103) is a dielectric material (column 4, lines 51-53).

8. As to claim 4, Hussein discloses that the thin film (103) is a low-k dielectric material (column 4, lines 60-67).

9. As to claim 5, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

10. As to claim 6, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

11. As to claim 11, Hussein discloses that the barrier material (108) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 10, lines 55-60).

12. As to claim 13, Hussein discloses that the step of filling the first pattern shape (106) with a conductive material (column 8, lines 65-66; Figure 1H) after removing the imaging material (136), the anti-reflective coating (108) and the planarizing material (104).

13. As to claim 14, Hussein discloses that the conductive material comprises copper (column 8, lines 65-66, column 10, lines 30-31).

14. As to claim 15, Hussein discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (103) on the substrate (100) (column 4, lines 51-53; Figure 1B); forming at least one via (107) in said dielectric material (103) (column 5, lines 14-15), such that at least one of the vias is positioned over the patterned conductor (Figure 1C); depositing a layer of planarizing material (104) on the dielectric material (103) and in the via (107) (column 5, lines 43-45); depositing a layer of anti-reflective coating (108) (column 10, lines 46-47, lines 55-60; Figure 3B); depositing at least one layer of imaging material (136) (column 6, lines 65-67; Figure 3C); forming at least one trench (106) in the layers of imaging material (136), anti-reflective coating (108) and planarizing material (104) (column 11, lines 19-22; Figures 1E-F), such that at least one of the trenches (106) is positioned over the via (107) (Figure 1F); removing the imaging material (136), either after or concurrently with forming the trench (106) in the planarizing material (104) (column 11, lines 23-24); removing the anti-reflective coating (108), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 31-35); transferring the at least one trench to the dielectric material (103), such that at least one of the trenches (106) is positioned over the via (107) (column 11, lines 19-22; Figure 1F).

15. Hussein does not expressly disclose depositing a layer of barrier material that substantially blocks impurity diffusion from the dielectric material into an imaging

material on the layer of planarizing material. Hussein discloses the use of both an imaging material (136) (column 6, lines 65-67) and low-k dielectric thin film (103) (column 4, lines 60-67). Tsai teaches that outgassing from a low-k dielectric film interacts with the imaging layer, resulting in the poisoning of via holes (column 5, lines 1-15; column 6, lines 12-28). To prevent poisoning, Tsai further teaches depositing a layer of barrier material (250) (column 6, lines 34-44; Figure 2C) that substantially blocks impurity diffusion from the dielectric material into an imaging material (column 5, lines 10-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a layer of barrier material that substantially blocks impurity diffusion from the dielectric material into an imaging material on the layer of planarizing material and to modify Hussein's method to account for the barrier material. One who is skilled in the art would be motivated to prevent the deleterious effects of via poisoning.

16. As to claim 16, Hussein discloses that the dielectric material (103) is a low-k dielectric material (column 4, lines 60-67).

17. As to claim 17, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

18. As to claim 18, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

19. As to claim 24, Tsai discloses that the barrier material (250) is silicon dioxide (column 6, lines 41-42).

20. As to claim 27, Tsai discloses that the barrier material (250) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 6, lines 39-44).

21. As to claim 29, Hussein discloses the step of filling the via (107) and the trench (106) with a conductive material (column 8, lines 65-66; Figure 1H), after removing the imaging material (136), the anti-reflective coating (108) and the planarizing material (104).

22. As to claim 30, Hussein discloses that the conductive material comprises copper (column 8, lines 65-66, column 10, lines 30-31).

23. As to claim 31, Hussein discloses that at least one via (107) has a height, and the layer of planarizing material (104) has a thickness of about half the via height to about twice the via height. Hussein discloses that dielectric material (103) has a minimum thickness of 2,000 Å (column 4, lines 66-67) and that via (107) is etched through the entire thickness of the dielectric material (column 5, lines 14-15). Hussein further discloses that planarizing material (104) has a thickness between 500 and 3,000 Å (column 5, lines 46-48).

24. As to claim 32, Tsai does not expressly disclose that the layer of barrier material (250) has a thickness of about 50 to 100 nm. However, Tsai discloses a barrier material thickness of 5 to 40 nm (column 6, lines 37-44), which is close enough to the Applicants' claimed thickness, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layer of barrier material with a thickness of about 50 to 100 nm. One who is

skilled in the art would be motivated to form the barrier layer at thickness known to prevent poisoning.

25. As to claim 33, Hussein discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (203) on the substrate (200) (Figure 2A); forming at least one trench (206) in the dielectric material (203) (column 9, lines 10-12), such that at least one of the trenches (206) is positioned over the patterned conductor (201) (Figure 2B); depositing a layer of planarizing material (204) on the dielectric material (203) and in the trench (column 9, lines 29-32; Figure 2C); depositing at least one layer of imaging material (250) (column 9, lines 37-38); forming at least one via in the layers of imaging material and planarizing material (column 9, lines 38-40), such that at least one of the via is positioned over the trench and the patterned conductor (Figure 2D); removing the imaging material (250), either after or concurrently with forming the via in the planarizing material (column 9, lines 64-67); transferring the at least one via (207) to the dielectric material (203), such that at least one of the via is positioned over the trench and the patterned conductor (column 9, lines 38-40; Figure 2E); and removing the planarizing material (column 9, lines 64-67).

26. Hussein does not expressly disclose, for the same embodiment, depositing a layer of anti-reflective coating on the layer of planarizing material; and removing the anti-reflective coating, either after or concurrently with transferring the at least one via to the dielectric material. However, for a different embodiment, Hussein discloses forming

a silicon nitride or titanium nitride (column 10, lines 55-60) inorganic anti-reflective layer (108) over planarizing layer (104) (column 10, lines 46-67). Furthermore, inorganic anti-reflective layer (108) is removed (column 11, lines 15-19) either after or concurrently with transferring the at least one feature to the dielectric material (column 11, lines 19-22). Moreover, the purpose of the anti-reflective coating is to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimension control (column 10, lines 61-67). Therefore, it would have been obvious to one of ordinary skill in art at the time the invention was made to deposit a layer of anti-reflective coating, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material. One who is skilled in the art would be motivated to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimensions.

27. Hussein does not expressly disclose depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric material into an imaging material on the layer of planarizing material. Hussein discloses the use of both an imaging material (136) (column 6, lines 65-67) and low-k dielectric thin film (103) (column 4, lines 60-67). Tsai teaches that outgassing from a low-k dielectric film interacts with the imaging layer, resulting in the poisoning of via holes (column 5, lines 1-15; column 6, lines 12-28). To prevent poisoning, Tsai further teaches depositing a layer of barrier material (250) (column 6, lines 34-44; Figure 2C) that substantially

blocks impurity diffusion from an underlying interlevel dielectric material into an imaging material (column 5, lines 10-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric material into an imaging material on the layer of planarizing material and to modify Hussein's method to account for the barrier material. One who is skilled in the art would be motivated to prevent the deleterious effects of via poisoning.

28. As to claim 34, Hussein discloses that the dielectric material (203) is a low-k dielectric material (column 9, lines 6-10; column 4, lines 60-67).

29. As to claim 35, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 9, lines 6-10; column 4, lines 60-67).

30. As to claim 36, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 9, lines 6-10; column 4, lines 60-67).

31. As to claim 42, Tsai discloses that the barrier material (250) is silicon dioxide (column 6, lines 41-42).

32. As to claim 45, Tsai discloses that the barrier material (250) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 6, lines 39-44).

33. As to claim 47, Hussein discloses the step of filling the via (207) and the trench (206) with a conductive material (column 10, lines 29-31; Figure 2G), after removing the imaging material (250), the anti-reflective coating (108) and the planarizing material (204).

34. As to claim 48, Hussein discloses that the conductive material comprises copper (column 10, lines 30-31).

35. As to claim 49, Tsai does not expressly discloses that the layer of barrier material (250) has a thickness of about 50 to 100 nm. However, Tsai discloses a barrier material thickness of 5 to 40 nm (column 6, lines 37-44), which is close enough to the Applicants' claims thickness, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layer of barrier material with a thickness of about 50 to 100 nm. One who is skilled in the art would be motivated to form the barrier layer at thickness known to prevent poisoning.

36. As to claim 52, Hussein discloses a method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of: depositing a thin film (103) on the substrate (100) (column 4, lines 51-53; Figure 1B); depositing a layer of planarizing material (104) on the thin film (103) (column 5, lines 43-51; Figure 1D); depositing at least one layer of imaging material (136) (column 6, lines 65-67; Figure 3C); forming at least one first pattern shape (106) in the layers of imaging material (136) and planarizing material (104) (column 11, lines 19-22; Figures 1E-F); removing the imaging material (136), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 23-24); and transferring the first pattern shape to the thin film (103) (column 11, lines 19-22; Figures 1E-F).

37. Hussein does not expressly disclose depositing a layer of barrier material of silicon oxide on the layer of planarizing material. Hussein discloses the use of both an

imaging material (136) (column 6, lines 65-67) and low-k dielectric thin film (103) (column 4, lines 60-67). Tsai teaches that outgassing from a low-k dielectric film interacts with the imaging layer, resulting in the poisoning of via holes (column 5, lines 1-15; column 6, lines 12-28). To prevent poisoning, Tsai further teaches depositing a layer of silicon oxide barrier material (250) (column 6, lines 34-44; Figure 2C) that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material (column 5, lines 10-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made depositing a layer of barrier material of silicon oxide on the layer of planarizing material and to modify Hussein's method to account for the silicon oxide barrier material. One who is skilled in the art would be motivated to prevent the deleterious effects of via poisoning.

38. As to claim 53, Hussein discloses that at least one second pattern shape (107) is formed in the thin film (103) prior to depositing the layer of planarizing material (104) (column 5, lines 14-15), and the second pattern shape (107) is filled by the planarizing material (104) (column 5, lines 43-45).

39. As to claim 54, Hussein discloses that the thin film (103) is a dielectric material (column 4, lines 51-53).

40. As to claim 55, Hussein discloses that the thin film (103) is a low-k dielectric material (column 4, lines 60-67).

41. As to claim 56, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

42. As to claim 57, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

43. As to claim 62, Hussein discloses depositing a layer of anti-reflective coating (108) prior to depositing the layer of imaging material (136) (column 10, lines 46-47, lines 55-60; Figure 3B); and removing the anti-reflective coating (108), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 31-35).

44. As to claim 63, Hussein discloses that the step of filling the first pattern shape (106) with a conductive material (column 8, lines 65-66; Figure 1H) after removing the imaging material (136), the anti-reflective coating (108) and the planarizing material (104).

45. As to claim 64, Hussein discloses that the conductive material comprises copper (column 8, lines 65-66, column 10, lines 30-31).

46. As to claim 66, Hussein discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (103) on the substrate (100) (column 4, lines 51-53; Figure 1B); forming at least one via (107) in said dielectric material (103) (column 5, lines 14-15), such that at least one of the vias is positioned over the patterned conductor (Figure 1C); depositing a layer of planarizing material (104) on the dielectric material (103) and in the via (107) (column 5, lines 43-45); depositing at least one layer of imaging material (136) (column 6, lines 65-67; Figure 3C); forming at least one trench (106) in the layers of imaging material (136), and

planarizing material (104) (column 11, lines 19-22; Figures 1E-F), such that at least one of the trenches (106) is positioned over the via (107) (Figure 1F); removing the imaging material (136), either after or concurrently with forming the trench (106) in the planarizing material (104) (column 11, lines 23-24); transferring the at least one trench to the dielectric material (103), such that at least one of the trenches (106) is positioned over the via (107) (column 11, lines 19-22; Figure 1F).

47. Hussein does not expressly disclose depositing a layer of barrier material of silicon oxide on the layer of planarizing material. Hussein discloses the use of both an imaging material (136) (column 6, lines 65-67) and low-k dielectric thin film (103) (column 4, lines 60-67). Tsai teaches that outgassing from a low-k dielectric film interacts with the imaging layer, resulting in the poisoning of via holes (column 5, lines 1-15; column 6, lines 12-28). To prevent poisoning, Tsai further teaches depositing a layer of silicon oxide barrier material (250) (column 6, lines 34-44; Figure 2C) that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material (column 5, lines 10-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made depositing a layer of barrier material of silicon oxide on the layer of planarizing material and to modify Hussein's method to account for the silicon oxide barrier material. One who is skilled in the art would be motivated to prevent the deleterious effects of via poisoning.

48. As to claim 67, Hussein discloses that the dielectric material (103) is a low-k dielectric material (column 4, lines 60-67).

49. As to claim 68, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

50. As to claim 69, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

51. As to claim 77, Hussein discloses depositing a layer of anti-reflective coating (108) prior to the deposition of the layer of imaging material (column 10, lines 46-47, lines 55-60; Figure 3B); and removing the anti-reflective coating (108), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 31-35).

52. As to claim 78, Hussein discloses the step of filling the via (207) and the trench (206) with a conductive material (column 10, lines 29-31; Figure 2G), after removing the imaging material (250) and the planarizing material (204).

53. As to claim 79, Hussein discloses that the conductive material comprises copper (column 10, lines 30-31).

54. As to claim 80, Hussein discloses that at least one via (107) has a height, and the layer of planarizing material (104) has a thickness of about half the via height to about twice the via height. Hussein discloses that dielectric material (103) has a minimum thickness of 2,000 Å (column 4, lines 66-67) and that via (107) is etched through the entire thickness of the dielectric material (column 5, lines 14-15). Hussein further discloses that planarizing material (104) has a thickness between 500 and 3,000 Å (column 5, lines 46-48).

55. As to claim 81, Tsai does not expressly disclose that the layer of barrier material (250) has a thickness of about 50 to 100 nm. However, Tsai discloses a barrier material thickness of 5 to 40 nm (column 6, lines 37-44), which is close enough to the Applicants' claims thickness, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layer of barrier material with a thickness of about 50 to 100 nm. One who is skilled in the art would be motivated to form the barrier layer at thickness known to prevent poisoning.

56. Claims 7-8, 20-23, 38-41, 58-59, and 71-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein, in view of Tsai, in further view of Lamb III et al. (U.S. Patent No. 6,391,472).

57. As to claims 7, 20, 38, 58, and 71 Hussein does not expressly disclose that the planarizing material is a poly(hydroxystyrene)-based system. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a poly(hydroxystyrene)-based system as a planarizing material. One who is skilled in the

art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

58. As to claims 8, 23, 41, 59, and 74, Hussein does not disclose that planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene, polycarbonates, epoxies, and polyesters (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a planarizing material selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

59. As to claims 21, 39, and 72, Hussein does not expressly disclose the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after

deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). It should be noted that there is a substantial overlap between Lamb's temperature range and the Applicants' range. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 200°C to about 250°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

60. As to claims 22, 40, and 73, Hussein does not disclose the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). Applicants' temperature is close enough to Lamb's temperature range, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 225°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

61. Claims 9-10, 19, 25-26, 37, 43-44, 50-51, 60-61, 65, 70, 75-76, 82-87, and 92-96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein, in view of Tsai, in view further view of Wolf, *Silicon Processing for the VLSI Era*, vols. 1 and 4, Lattice Press (1986, 2002).

62. As to claims 9, 25, 43, 60, 75, and 92, Tsai discloses that barrier material comprises silicon dioxide (column 6, lines 34-44). Tsai does not expressly disclose that silicon oxide deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). It should be noted that the Applicants' temperature range overlaps with the typical temperature taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit silicon nitride by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. One who is skilled in the art would be motivated to use an established method for depositing oxide and select deposition temperatures that either overlap or are similar to conventional temperatures.

63. As to claims 10, 26, 44, 61, 76, and 93, Tsai does not expressly discloses that the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2,

page 183). Although Applicants' temperature range is outside the typical temperature taught by Wolf, the temperatures are close enough, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the barrier material deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. One who is skilled in the art would be motivated to select an established method for depositing oxide and to select a deposition temperature that is similar to a conventional temperature.

64. As to claims 19, 37, 70, and 87, Hussein does not expressly disclose that the low-k dielectric material is SiCOH deposited by chemical vapor deposition. However, Wolf teaches that SiCOH, deposited by chemical vapor deposition, is a commonly used low-k dielectric material (vol. 4, page 690) for damascene structures (vol. 4, page 689). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SiCOH as the low-k dielectric material, deposited by chemical vapor deposition. One who is skilled in the art would be motivated to use a commonly used low-k material, which has been successfully implemented for producing damascene structures.

65. As to claims 50, Hussein discloses removing the planarizing material (column 9, lines 64-67). Hussein does not expressly disclose removing the barrier material, either after or concurrently with transferring the at least the first shape pattern to the thin film. However, Hussein discloses the removal of all materials from the first shape pattern (106) after the first shape pattern is etched (column 7, lines 62-67; column 8, lines 1-12)

in a low-k dielectric (column 4, lines 60-67). Wolf teaches that if a higher-k dielectric (such as a barrier material) remains embedded with a low-k dielectric, the net k of the stack increase (vol. 4, page 680). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the barrier material, either after or concurrently with transferring the at least the first shape pattern to the thin film. One who is skilled in the art would be motivated to prevent any increase in the dielectric constant of the dielectric stack.

66. As to claim 51, Hussein discloses removing the planarizing material (column 9, lines 64-67). Hussein does not expressly disclose removing the barrier material, either after or concurrently with transferring the at least the one trench to the dielectric material. However, Hussein discloses the removal of all materials from the trench (106) after the trench is etched (column 7, lines 62-67; column 8, lines 1-12) in a low-k dielectric (column 4, lines 60-67). Wolf teaches that if a higher-k dielectric (such as a barrier material) remains embedded with a low-k dielectric, the net k of the stack increase (vol. 4, page 680). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the barrier material, either after or concurrently with transferring the at least the one trench to the dielectric material. One who is skilled in the art would be motivated to prevent any increase in the dielectric constant of the dielectric stack.

67. As to claim 65, Hussein discloses removing the planarizing material (column 9, lines 64-67). Hussein does not expressly disclose removing the silicon dioxide, either after or concurrently with transferring the at least the first shape pattern to the thin film.

However, Hussein discloses the removal of all materials from the first shape pattern (106) after the first shape pattern is etched (column 7, lines 62-67; column 8, lines 1-12) in a low-k dielectric (column 4, lines 60-67). Wolf teaches that if a higher-k dielectric (such as silicon dioxide) remains embedded with a low-k dielectric, the net k of the stack increase (vol. 4, page 680). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the silicon dioxide, either after or concurrently with transferring the at least the first shape pattern to the thin film. One who is skilled in the art would be motivated to prevent any increase in the dielectric constant of the dielectric stack.

68. As to claim 82, Hussein discloses removing the planarizing material (column 9, lines 64-67). Hussein does not expressly disclose removing the silicon dioxide, either after or concurrently with transferring the at least the at least one trench to the dielectric material. However, Hussein discloses the removal of all materials from the trench (106) after the trench is etched (column 7, lines 62-67; column 8, lines 1-12) in a low-k dielectric (column 4, lines 60-67). Wolf teaches that if a higher-k dielectric (such as silicon dioxide) remains embedded with a low-k dielectric, the net k of the stack increase (vol. 4, page 680). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the silicon dioxide, either after or concurrently with transferring the at least the at least one trench to the dielectric material. One who is skilled in the art would be motivated to prevent any increase in the dielectric constant of the dielectric stack.

69. As to claim 83, Hussein discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (203) on the substrate (200) (Figure 2A); forming at least one trench (206) in the dielectric material (203) (column 9, lines 10-12), such that at least one of the trenches (206) is positioned over the patterned conductor (201) (Figure 2B); depositing a layer of planarizing material (204) on the dielectric material (203) and in the trench (column 9, lines 29-32; Figure 2C); depositing a layer of anti-reflective coating (108) (column 10, lines 46-47, lines 55-60; Figure 3B); depositing at least one layer of imaging material (250) (column 9, lines 37-38); forming at least one via in the layers of imaging material and planarizing material (column 9, lines 38-40), such that at least one of the via is positioned over the trench and the patterned conductor (Figure 2D); removing the imaging material (250), either after or concurrently with forming the via in the planarizing material (column 9, lines 64-67); transferring the at least one via (207) to the dielectric material (203), such that at least one of the via is positioned over the trench and the patterned conductor (column 9, lines 38-40; Figure 2E); and removing the planarizing material (column 9, lines 64-67).

70. Hussein does not expressly disclose depositing a layer of barrier material of silicon oxide on the layer of planarizing material. Hussein discloses the use of both an imaging material (136) (column 6, lines 65-67) and low-k dielectric thin film (103) (column 4, lines 60-67). Tsai teaches that outgassing from a low-k dielectric film interacts with the imaging layer, resulting in the poisoning of via holes (column 5, lines

1-15; column 6, lines 12-28). To prevent poisoning, Tsai further teaches depositing a layer of silicon oxide barrier material (250) (column 6, lines 34-44; Figure 2C) that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material (column 5, lines 10-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made depositing a layer of barrier material of silicon oxide on the layer of planarizing material and to modify Hussein's method to account for the silicon oxide barrier material. One who is skilled in the art would be motivated to prevent the deleterious effects of via poisoning.

71. Hussein does not expressly disclose removing the barrier material, either after or concurrently with transferring the at least the at least one via to the dielectric material. However, Hussein discloses the removal of all materials from the via (209) after the via is etched (column 9, lines 64-67; column 10, lines 1-11) in a low-k dielectric (column 4, lines 60-67). Wolf teaches that if a higher-k dielectric (such as silicon dioxide) remains embedded with a low-k dielectric, the net k of the stack increase (vol. 4, page 680). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the barrier material, either after or concurrently with transferring the at least the at least one via to the dielectric material. One who is skilled in the art would be motivated to prevent any increase in the dielectric constant of the dielectric stack.

72. As to claim 84, Hussein discloses that the thin film (103) is a low-k dielectric material (column 4, lines 60-67).

73. As to claim 85, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

74. As to claim 86, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

75. As to claim 94, Hussein discloses depositing a layer of anti-reflective coating (108) prior to depositing the layer of imaging material (136) (column 10, lines 46-47, lines 55-60; Figure 3B); and removing the anti-reflective coating (108), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 31-35).

76. As to claim 95, Hussein discloses the step of filling the via (207) and the trench (206) with a conductive material (column 10, lines 29-31; Figure 2G), after removing the imaging material (250) and the planarizing material (204).

77. As to claim 96, Hussein discloses that the conductive material comprises copper (column 10, lines 30-31).

78. As to claim 97, Tsai does not expressly discloses that the layer of barrier material (250) has a thickness of about 50 to 100 nm. However, Tsai discloses a barrier material thickness of 5 to 40 nm (column 6, lines 37-44), which is close enough to the Applicants' claims thickness, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layer of barrier material with a thickness of about 50 to 100 nm. One who is skilled in the art would be motivated to form the barrier layer at thickness known to prevent poisoning.

79. Claims 88-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein, in view of Tsai, in view further view of Wolf, in further view of Lamb III.

80. As to claim 88 Hussein does not expressly disclose that the planarizing material is a poly(hydroxystyrene)-based system. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a poly(hydroxystyrene)-based system as a planarizing material. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

81. As to claim 89, Hussein does not expressly disclose the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). It should be noted that there is a substantial overlap between Lamb's temperature range and the Applicants' range. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to incorporate the step of baking the planarizing material at a temperature of about 200°C to about 250°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

82. As to claim 90, Hussein does not disclose the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). Applicants' temperature is close enough to Lamb's temperature range, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 225°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature

83. As to claim 91, Hussein does not disclose that planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during

etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene, polycarbonates, epoxies, and polyesters (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a planarizing material selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

Response to Arguments

84. Applicants' arguments (Applicants' Remarks, pages 20-25), filed Aug. 4, 2005, with respect to the rejection of claims 1-6, 11, 13-18, 27, 29-32 and 50-51 under 35 U.S.C. 102(b)/103(a) in view of Hussein have been fully considered and are persuasive. As to claims 1 and 15, Applicants have correctly pointed out that Hussein does not disclose the features of: depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material and depositing a layer of anti-reflective coating on the layer of barrier material (pages 21-23). As to newly added claims 55 and 62, Applicants have also correctly pointed out that Hussein does not disclose that feature of depositing a

layer of barrier material of silicon oxide on the layer of planarizing material (pages 23-25). Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Hussein and Tsai.

85. Applicants' arguments (Applicants' Remarks, pages 26-27), filed Aug. 4, 2005, with respect to the rejection of claims 12, 28, 33-36, and 45-49 under 35 U.S.C. 103(a) as being unpatentable over Hussein have been fully considered and are persuasive. As to claim 33, Applicants have correctly pointed out that Hussein does not disclose the features of depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material and depositing a layer of anti-reflective coating on the layer of barrier material (page 27). Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Hussein and Tsai.

86. Applicants' arguments (Applicants' Remarks, page 28), filed Aug. 4, 2005, with respect to the rejection of claims 7-8, 20-23, and 38-41 under 35 U.S.C. 103(a) as being unpatentable over Hussein, in view of Lamb III, have been fully considered and are persuasive, as discussed above. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Hussein and Tsai.

87. Applicants' arguments (Applicants' Remarks, page 29), filed Aug. 4, 2005, with respect to the rejection of claims 9-10, 19, 24-26, 37, and 42-44 under 35 U.S.C. 103(a) as being unpatentable over Hussein, in view of Wolf, have been fully considered and

are persuasive, as discussed above. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Hussein and Tsai.

88. Applicants' arguments (Applicants' Remarks, page 30), filed Aug. 4, 2005, with respect to the rejection of claims 33-36, 42, 45, and 47-49 under 35 U.S.C. 103(a) as being unpatentable over Daniels have been fully considered and are persuasive. Applicants have correctly pointed out that Daniels does not disclose depositing a layer of anti-reflective coating on the layer of barrier material (page 30). Therefore, the rejection has been withdrawn.

89. Applicants' arguments (Applicants' Remarks, page 31), filed Aug. 4, 2005, with respect to the rejection of claims 38-41under 35 U.S.C. 103(a) as being unpatentable over Daniels, in view of Lamb III, have been fully considered and are persuasive, as discussed above. Therefore, the rejection has been withdrawn.

Conclusion

90. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC
Aug. 29, 2005

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SUPERVISORY PATENT EXAMINER